What is claimed is:

1. A memory array for a DRAM chip with open bit-line architecture, comprising:

a plurality of gate-lines, each gate-line having a loop portion with a first segment and a second segment; and

a plurality of DRAM cells associated with each gate-line and having first DRAM cells and second DRAM cells, wherein the first DRAM cells have first gates consisting of the first segment and the second DRAM cells have second gates consisting of the second segment; and

a plurality of bit-lines connected with the DRAM cells, each of the bit-lines is connected to either one of the first DRAM cells or one of the second DRAM cells.

2. The memory array as claimed in claim 1, wherein the gate-lines are defined and formed by using an alternating phase-shift mask in conjunction with a single exposure process.

3. The memory array as claimed in claim 1, wherein the first and the second DRAM cell have active areas defined by a dark loop on a mask.

4. The memory array as claimed in claim 3, wherein the mask is an alternating phase-shift mask and, during a lithography process, first light traversing a first portion enclosed by the dark loop and second light traversing a second portion adjacent the dark loop are 180 out of phase.

5. A alternating phase-shift mask for defining gate patterns on a DRAM chip with open bit-line architecture, comprising:

opaque lines for defining gate-lines of a memory array in the DRAM chip, each opaque line having:

a dark loop;

a first portion enclosed and defined by the dark loop; and

a second portion adjacent the dark loop;

wherein, during a lithography process, first light traversing the first portion and second light traversing the second portion are 180 out of phase.

6. A alternating phase shift mask for defining active areas on a DRAM chip, comprising:

opaque lines for defining active areas of a memory array in the DRAM chip, each opaque line having:

a dark loop;

a first portion enclosed and defined by the dark loop; and

a second portion adjacent the dark loop;

wherein, during a lithography process, first light traversing the first portion and second light traversing the second portion are 180 out of phase.

7. A memory array for a DRAM chip, comprising:

a plurality of DRAM cells, arranged in rows and columns, wherein a first edging DRAM cell at one end of a first

row has a common active area shared with a second edging DRAM cell at one end of an adjacent row, the common active area is defined by a dark loop on an alternating phase-shft mask, and, during a lithography process, first light traversing a first portion enclosed by the drak loop portion and second light traversing a second portion adjacent the dark loop portion are 180 out of phase.

8. The memory array as claimed in the claim 7, further comprising:

a plurality of gate-lines, each gate-line having:

a loop portion with a first segment and a second segment; and

a plurality of bit-lines connected with the DRAM cells;

wherein the plurality of DRAM cells have first DRAM cells and second DRAM cells, the first DRAM cells have first gates consisting of the first segment, the second DRAM cells have second gates consisting of the second segment, and each of the bit-lines is connected to either one of the first DRAM cells or one of the second DRAM cells to construct open bit-line structure.

9. A method for manufacturing DRAM chips, comprising:

providing a first alternating phase-shift mask, having:

opaque lines, each opaque line having a dark loop;

a first portion enclosed and defined by the dark loop; and

a second portion adjacent the dark loop, wherein, during a lithography process, first light

traversing the first portion and second light traversing the second portion are 180 out of phase;

patterning, through the lithography process in together with the first alternating phase-shift mask, active areas of a memory array, wherein at least two edging DRAM cells in the memory array share a common active area.

10. A method for manufacturing DRAM chips, comprising:

providing a first alternating phase-shft mask, having:

opaque lines, each opaque line having a dark loop;

a first portion enclosed and defined by the dark loop; and

a second portion adjacent the dark loop, wherein, during a lithography process, first light traversing the first portion and second light traversing the second portion are 180 out of phase;

patterning, through the lithography process in together with the first alternating phase-shift mask, gate-lines of a memory array, wherein each gate-line has a loop portion corresponds to the dark loop on the first alternating phase-shft mask.